**EXPERIMENT NO:-6**

**➢ AIM:** To Design and test decoder circuit.

**➢ APPARATUS:** Logisim simulator

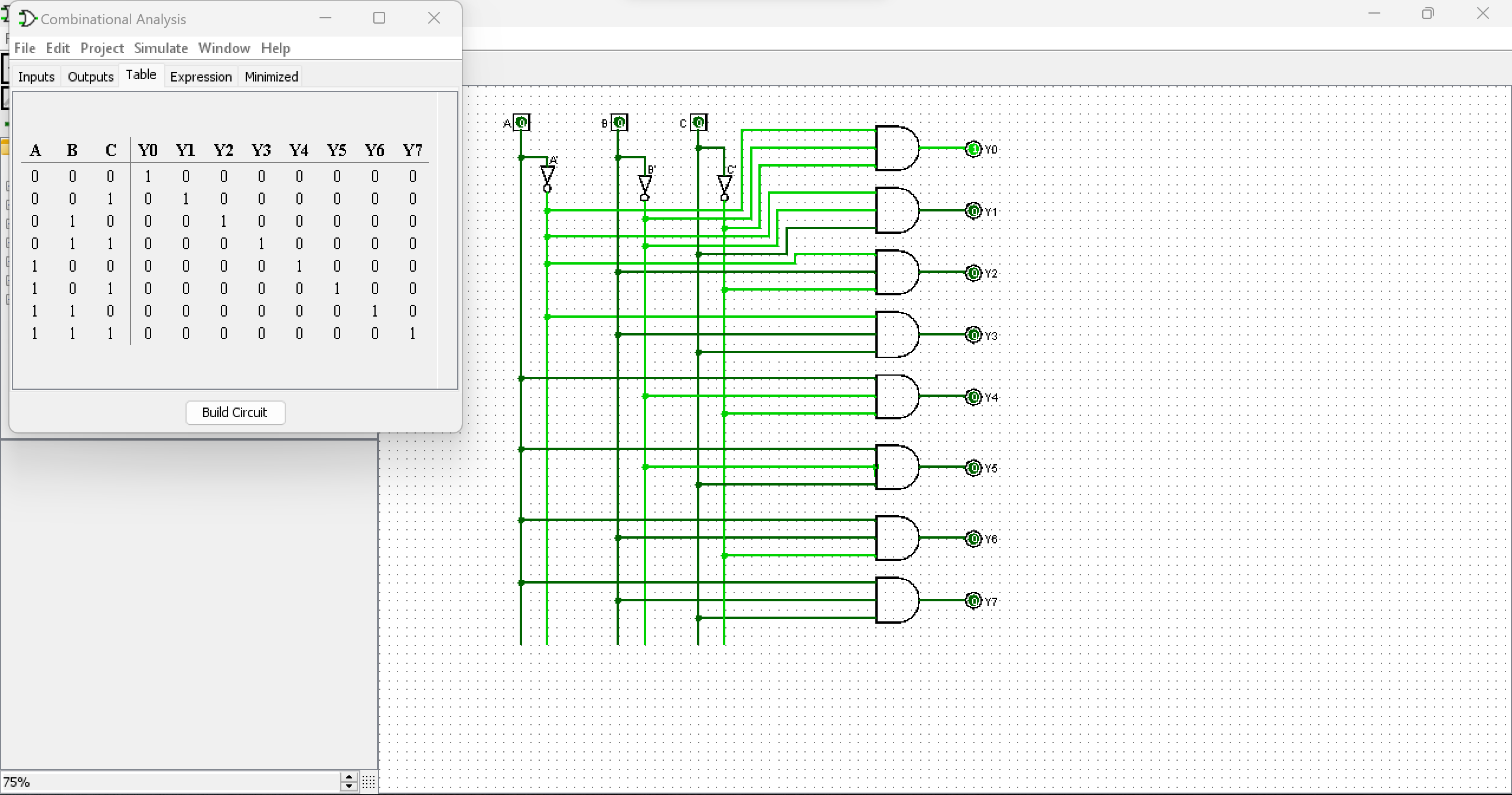
**➢ THEORY:**

Discrete quantities of information are represented in digital systems with binary codes.  
A binary code of n bits is capable of representing up to 2^n distinct elements of the coded  
information. A decoder is a combinational circuit that converts binary information from n input  
lines to a maximum of 2^n unique output lines. If the n-bit decoded information has unused or  
don’t-care combinations, the decoder output will have less than 2^n outputs.

The decoders presented here are called n-to-m line decoders where m<=2^n. Their  
purpose is to generate the 2^n (or less) minterms of n input variables. The name decoder is also  
used in conjunction with some code such as BCD-to seven -segment decoder.

Consider the 3 to 8 line decoder circuit. The three inputs are decoded into eight outputs.  
Each output representing one of the minterms of the 3-input variables. The three inverters  
provide the complement of the outputs, and each one of eight AND gates generate one of the  
minterms. A particular application of this decoder would be a binary to octal conversion. The  
input variables may represent a binary number, and the outputs will then represent the eight  
digits in the octal number system. However a 3-to-8-line decoder can be used for decoding and  
3-bit code to provide eight outputs, one for each element of the code.

CIRCUIT DIAGRAM OF 3 TO 8 BIT DECODER:



TRUTH TABLE OF 3 TO 8 BIT DECODER:

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **INPUTS** | | | | **OUTPUTS** | | | | | | | |
| **ENABLE** | **ADDRESS**  **LINES** | | |
| **EN** | **A** | **B** | **C** | **Y0** | **Y1** | **Y2** | **Y3** | **Y4** | **Y5** | **Y6** | **Y7** |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

**CONCLUSION -** Designing and testing a decoder circuit (using AND - NOT) is a fundamental exercise in digital electronics, providing practical experience and reinforcing key concepts in binary decoding and logic circuits.